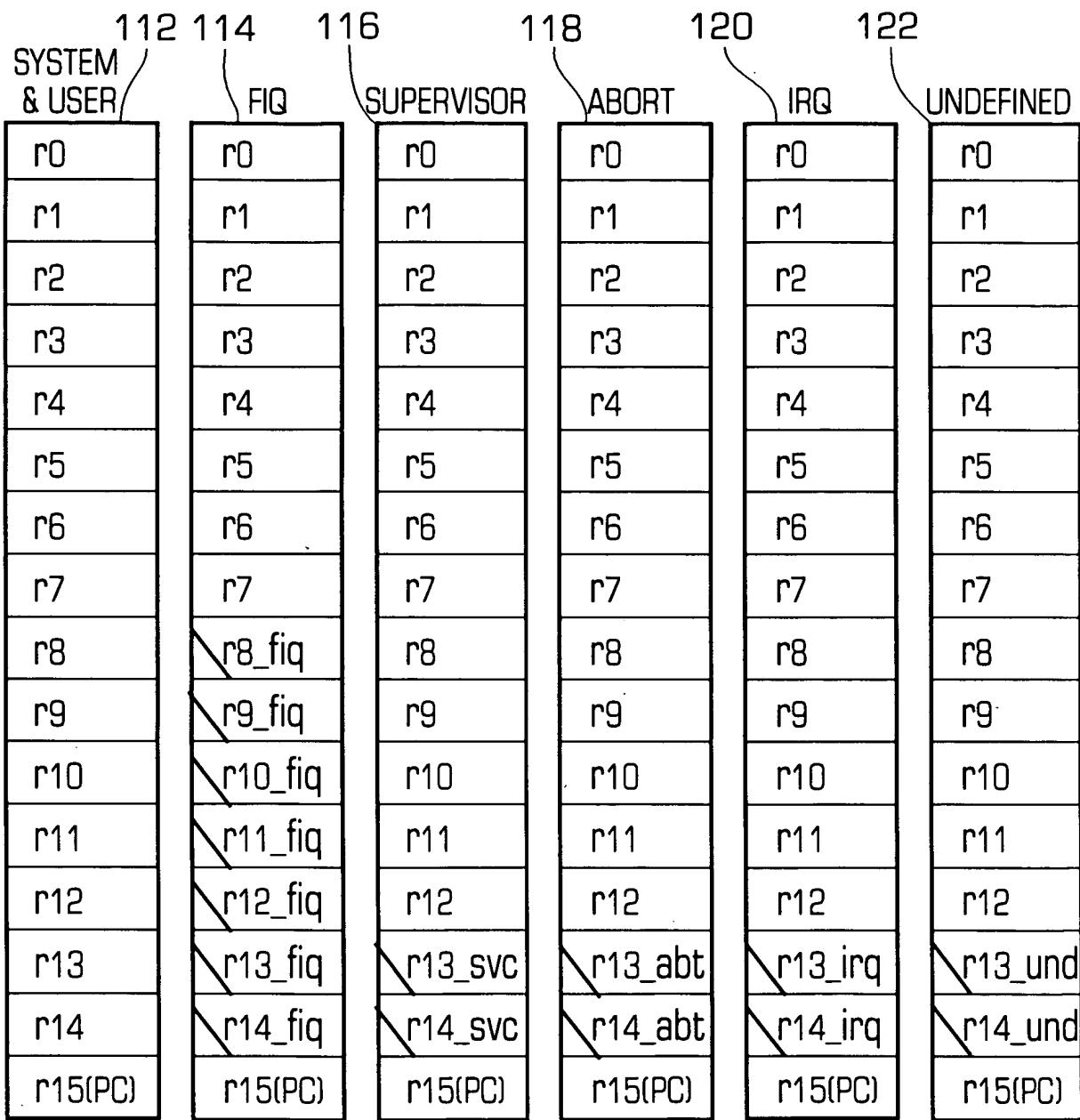


FIG. 1

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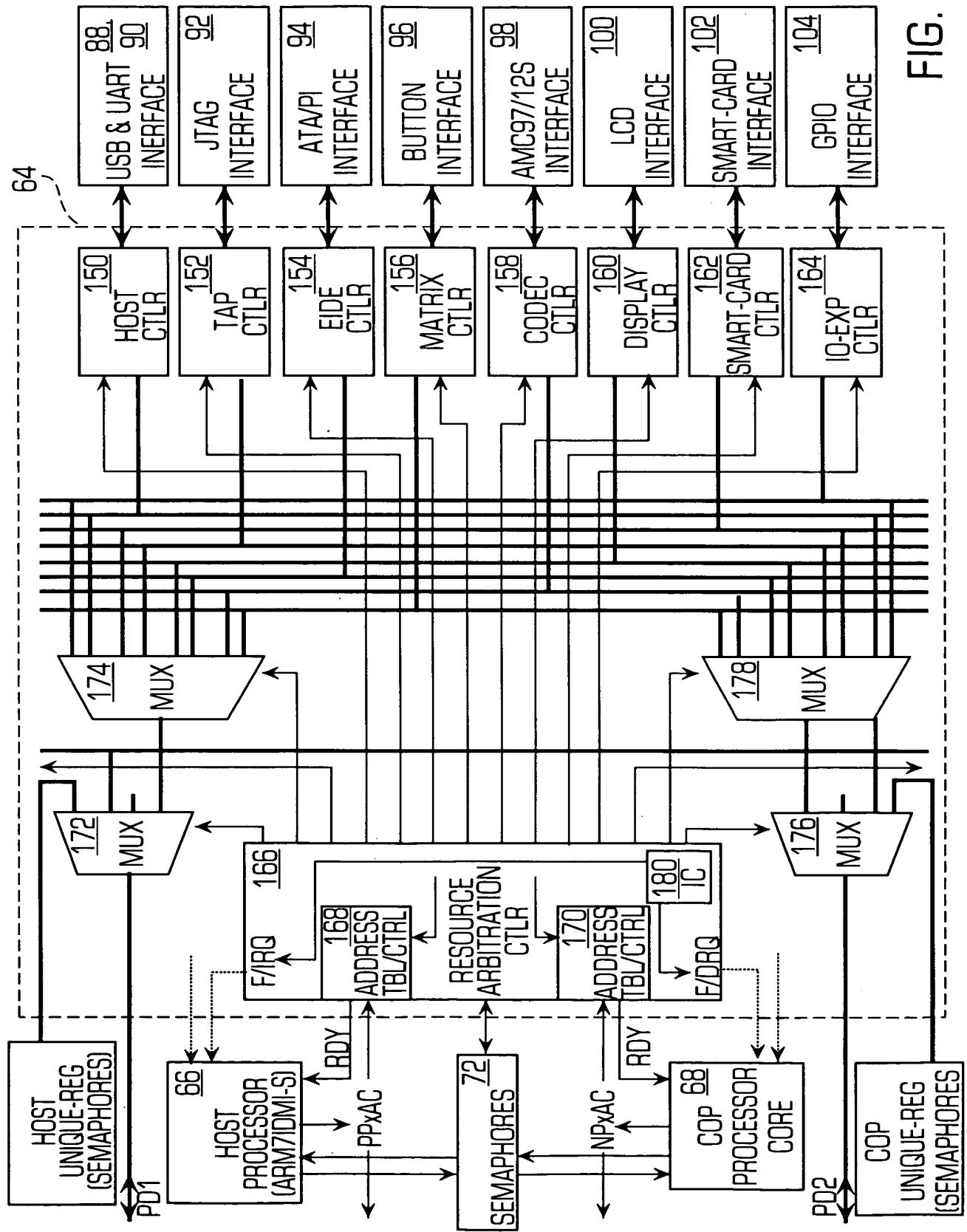


FIG. 3

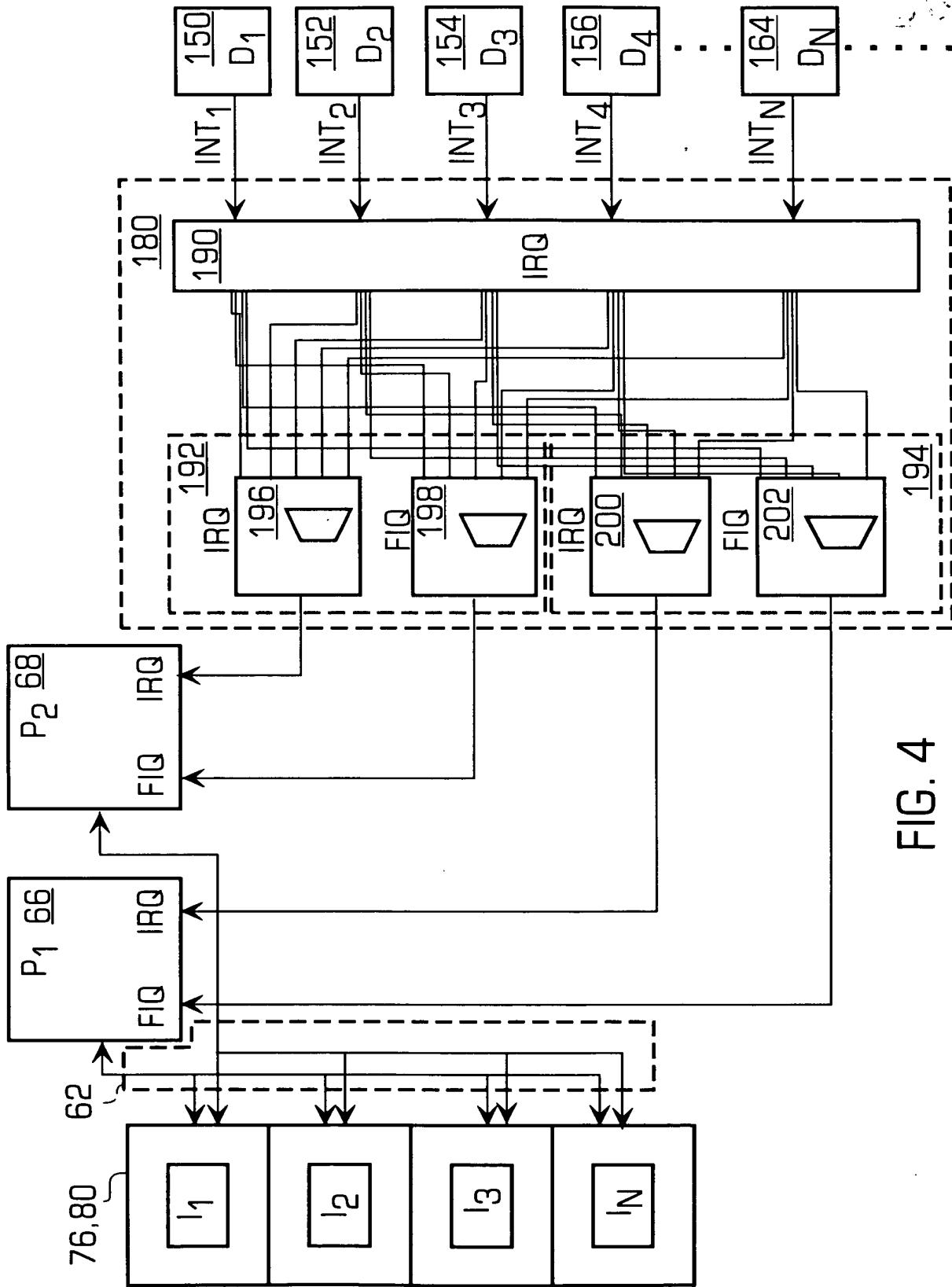


FIG. 4

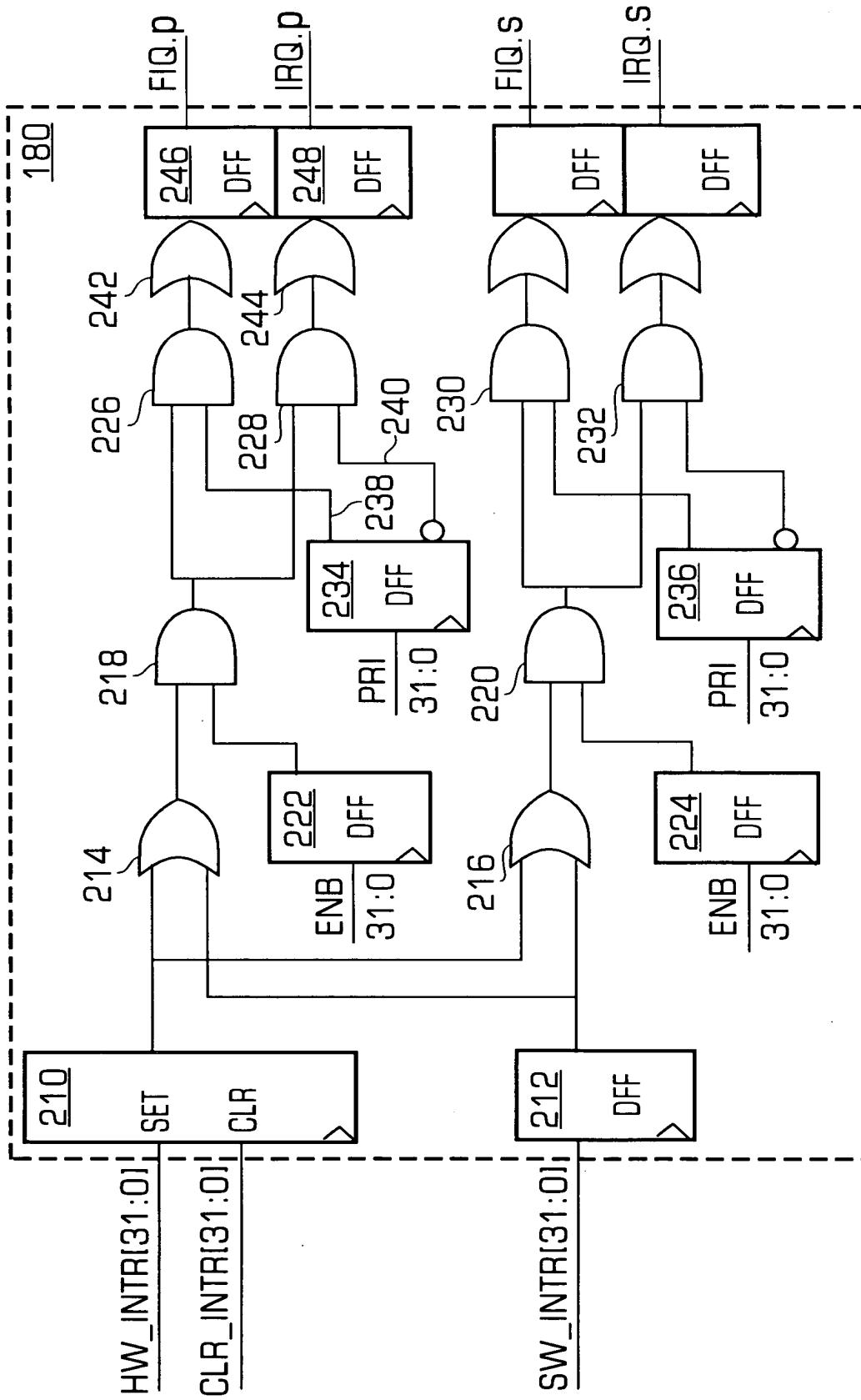
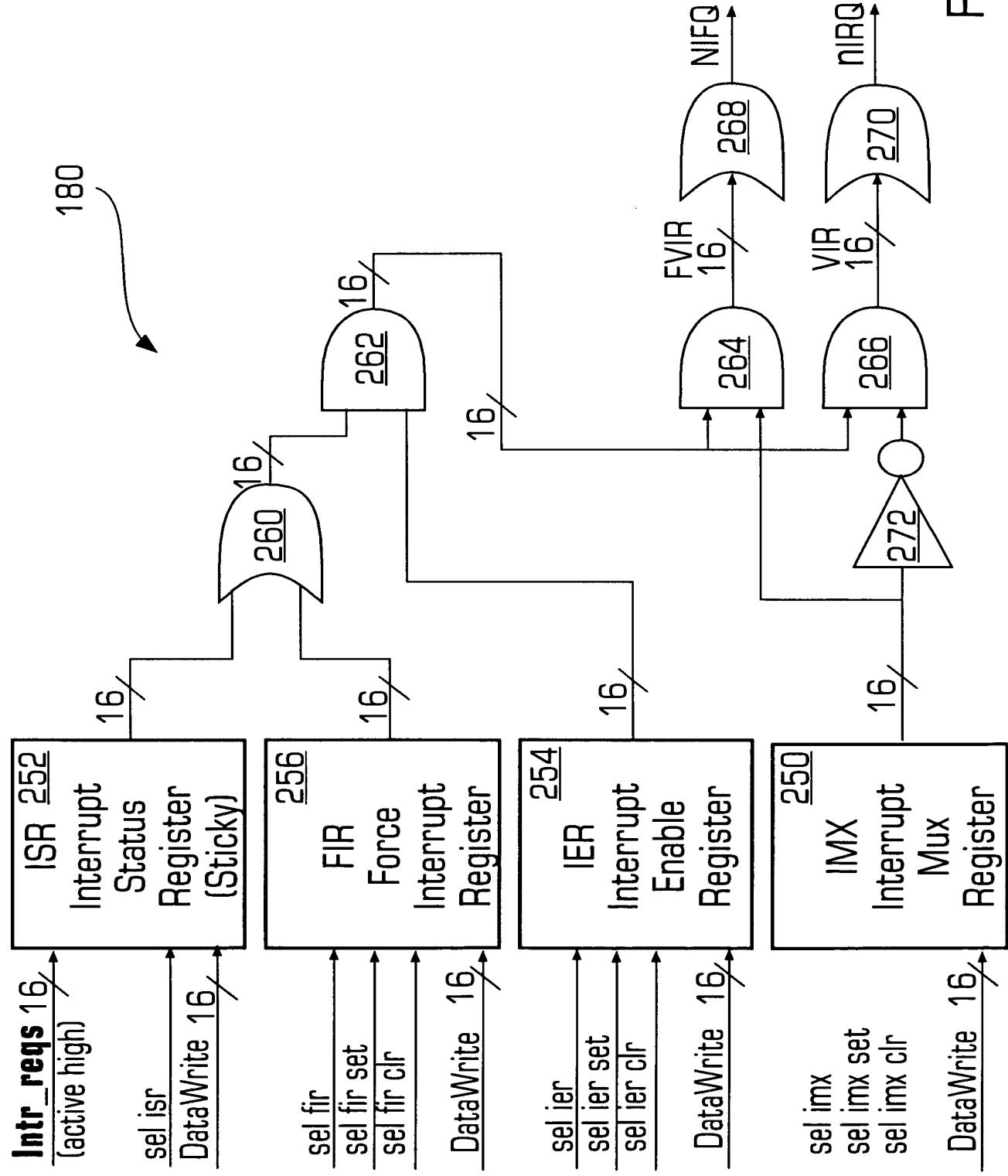


FIG. 5

FIG. 6



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Offset	Register	Description
0	ISR	Interrupt Status Register
4	IER	Interrupt Enable Register
8	IER_set	Each bit written as one will set the corresponding bit in IER
C	IER_clr	Each bit written as one will clr the corresponding bit in IER
10	FIR	Force Interrupt Register
14	FIR_set	Each bit written as one will set the corresponding bit in FIR
18	FIR_clr	Each bit written as one will clr the corresponding bit in FIR
1C	IMX	Interrupt Mux Register ('1/0' Routes interrupt to nFIQ/nIRQ)
20	IMX_set	Each bit written as one will set the corresponding bit in IMX
24	IMX_clr	Each bit written as one will clr the corresponding bit in IMX
28	VIR	Read only Valid Interrupt Register for nIRQ
2C	FVIR	Read only Fast Valid Interrupt Register for nFIQ

FIG. 7

Bit	Description
0	USB
1	UART A
2	UART B
3	External
4	USB Fast
5	Not Defined (CIF)
6	Not Defined
7	Not Defined (Keyboard)
8	EIDE 1
9	EIDE 2
A	Not Defined
B	Not Defined
C	Not Defined
D	Timer 2
E	Timer 1
F	Not defined
10	USB Reset
11	AC
12	Timer 1
13	Timer 2
31:14	Not Defined

FIG. 8

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INTERRUPT CONTROLLER				
VIRQ_CPU	CF00:1000	RO	32B	VALID INTERRUPT STATUS FOR CPU (PRIMARY)
VIRQ_COP	CF00:1004	RO	32B	VALID INTERRUPT STATUS FOR COP (SECONDARY)
VFIQ_CPU	CF00:1008	RO	32B	FIQ VALID INTERRUPT STATUS FOR CPU (PRIMARY)
VFIQ_COP	CF00:100C	RO	32B	FIQ VALID INTERRUPT STATUS FOR COP (SECONDARY)
ISR (READ-ONLY)	CF00:1010	RO	32B	LATCHED INTERRUPT STATUS REGISTER (HW)
FIR (READ-ONLY)	CF00:1014	RO	32B	FORCED INTERRUPT STATUS REGISTER (SW)
FIR_SET	CF00:1018	SET	32B	FORCE INTERRUPT REGISTER SET
FIR_CLR	CF00:101C	CLR	32B	FORCE INTERRUPT REGISTER CLEAR
CPU_IER (READ-ONLY)	CF00:1020	RO	32B	ENABLED INTERRUPT SOURCE FOR CPU
CPU_IER_SET	CF00:1024	SET	32B	SET INTERRUPT SOURCE FOR CPU
CPU_IER_CLR	CF00:1028	CLR	32B	CLEAR INTERRUPT SOURCE FOR CPU
CPU_IEP_CLASS	CF00:102C	RW	32B	CPU'S INTERRUPT ENABLE PRIORITY CLASS (FIQ/IRQ)
COP_IER (READ-ONLY)	CF00:1030	RO	32B	ENABLED INTERRUPT SOURCE FOR COP
COP_IER_SET	CF00:1034	SET	32B	SET INTERRUPT SOURCE FOR COP
COP_IER_CLR	CF00:1038	CLR	32B	CLEAR INTERRUPT SOURCE FOR COP
COP_IEP_CLASS	CF00:103C	RW	32B	COP'S INTERRUPT ENABLE PRIORITY CLASS (FIQ/IRQ)
DMA_STATUS	CF00:1040	RO	32B	DMA INTERRUPT SOURCE STATUS

FIG. 9A

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FIG. 9B

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IRQ15	IRQ14	IRQ13	IRQ12	IRQ11	IRQ10	IRQ9	IRQ8	IRQ7	IRQ6	IRQ5	IRQ4	IRQ3	IRQ2	IRQ1	IRQ0
IRQ15	IRQ14	IRQ13	IRQ12	IRQ11	IRQ10	IRQ9	IRQ8	IRQ7	IRQ6	IRQ5	IRQ4	IRQ3	IRQ2	IRQ1	IRQ0
FIQ15	FIQ14	FIQ13	FIQ12	FIQ11	FIQ10	FIQ9	FIQ8	FIQ7	FIQ6	FIQ5	FIQ4	FIQ3	FIQ2	FIQ1	FIQ0
FIQ15	FIQ14	FIQ13	FIQ12	FIQ11	FIQ10	FIQ9	FIQ8	FIQ7	FIQ6	FIQ5	FIQ4	FIQ3	FIQ2	FIQ1	FIQ0
FIQ15	FIQ14	FIQ13	FIQ12	FIQ11	FIQ10	FIQ9	FIQ8	FIQ7	FIQ6	FIQ5	FIQ4	FIQ3	FIQ2	FIQ1	FIQ0
ISR15	ISR14	ISR13	ISR12	ISR11	ISR10	ISR9	ISR8	ISR7	ISR6	ISR5	ISR4	ISR3	ISR2	ISR1	ISR0
FIR15	FIR14	FIR13	FIR12	FIR11	FIR10	FIR9	FIR8	FIR7	FIR6	FIR5	FIR4	FIR3	FIR2	FIR1	FIR0
FIR_SET (SET FORCED INTERRUPT BIT)															
FIR_CLR (CLEAR FORCED INTERRUPT BIT)															
IER15	IER14	IER13	IER12	IER11	IER10	IER9	IER8	IER7	IER6	IER5	IER4	IER3	IER2	IER1	IER0
CPU_IER_SET (ENABLE INTERRUPT SOURCE FOR CPU)															
CPU_IER_CLR (DISABLE INTERRUPT SOURCE FOR CPU)															
CPU-IEP_CLASS (SET PRIORITY INTERRUPT SOURCE FOR CPU)															
IER15	IER14	IER13	IER12	IER11	IER10	IER9	IER8	IER7	IER6	IER5	IER4	IER3	IER2	IER1	IER0
COP_IER_SET (ENABLE INTERRUPT SOURCE FOR COP)															
COP_IER_CLR (DISABLE INTERRUPT SOURCE FOR COP)															
COP_IEP_CLASS (SET PRIORITY INTERRUPT SOURCE FOR COP)															
DMA_SOURCE_STATUS															

FIG. 9C